REMARKS

I. Summary of the Examiner's Action

A. Claim Rejections

As set forth in paragraph 3 of the Office Action, claims 1, 2, 5, 6 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent Application No. 2002/0085657 A1 to Boerstler (hereinafter "the Boerstler application") and further in view of United States Patent No. 6,781,419 to Harrison (hereinafter "the Harrison patent").

As set forth in paragraph 4 of the Office Action, claims 3 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Boerstler application and Harrison patent as applied to the foregoing claims, and further in view United States Patent No. 3,629,712 to Clark (hereinafter "the Clark patent").

These rejections are respectfully disagreed with, and are traversed below.

B. Claim Objections and Allowable Subject Matter

At page 4, lines 16 – 18 of the Office Action the Examiner objected to claim 4 as being dependent upon a rejected base claim, but indicated that it would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

II. Applicant's Response – Claim Rejections

A. Rejection of Claims 1, 2, 5, 6 and 8 under 35 U.S.C. § 103(a)

Claim 1 recites the following subject matter (emphasis added):

> 1. A circuit for controlling the duty cycle and jitter of a clock signal, comprising:
>
> an input node for receiving the clock signal; and
>
> an output node for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle.

Applicant has carefully examined the Boerstler application and Harrison patent relied upon by the Examiner and has not located the foregoing underlined subject matter. In particular, it is not seen how the Boerstler application relates to the subject matter of the instant claim. In the Office Action dated July 28, 2005 (hereinafter "the July 28 Office Action") the Examiner states the following at page 2, lines 17 – 20:

> "Regarding claim 1, Boerstler discloses (figure 8):
> - An input node for receiving the clock signal (14); and
> - An output node for outputting a process clock signal (16) having a first edge that is synchronized to an edge of the clock signal (page 1, paragraph # 0014)."

Reading the Examiner's rejection one would think that Boerstler likely would describe or suggest a circuit that performs operations on a clock signal to create a modified clock

signal. The method of the Boerstler application, however, does not operate on a clock signal *per se*; rather, the Boerstler method derives a clock signal from an input data signal, and then re-synchronizes the data signal in accordance with the derived clock signal. The Boerstler patent does not generate a modified clock signal, but rather a modified *data signal*.

The operation of Boerstler's method is described at paragraph 14, which is reproduced here (emphasis added):

> "The foregoing objects are achieved in a method of extracting a clock signal from a data stream, generally comprising the steps of generating a plurality of multiphase clock signals, selecting one of the multiphase signals based on a plurality of synchronization states identifying which of the multiphase clock signals is most closely aligned with the data stream, and sampling the data stream using the selected one of the multiphase signals to produce a retimed data signal. The multiphase clock signals may be sub-harmonics of the data stream. The selecting step may include the determination of whether the multiphase clock signals are either early or late with respect to the data stream, particularly using D-type flip-flops. The synchronization states are used to define which of the rising edges of the multiphase clock signals is most closely aligned with an edge of the data stream. A multiphase voltage-controlled oscillator may be used to provide the multiphase clock signals. An error signal is created using the multiphase clock signals and the data stream which is applied to a charge pump, and the multiphase clock signals are corrected using a control voltage output of the charge pump."

The Boerstler application simply concerns totally different subject matter from Applicant's invention. The Boerstler method does not have "an input node for receiving the clock signal," but instead an input node for receiving a *data signal.* In addition, the Boerstler method does not output "a *processed clock signal*" but rather "a *retimed data signal.*" These differences, while determinative in and of themselves, are just the beginning. The Boerstler method derives a plurality of clock signals from the input data signal, and then selects the clock signal that is most closely aligned with the data signal. Applicant's apparatus simply does not operate in this manner. Applicant's apparatus as depicted in, and described with respect to FIG. 2, operates on clock signal (205A) and outputs a clock signal (207A). Multiple intermediate clock signals are not created in Applicant's invention as claimed.

In addition, the Examiner indicates that reference numeral 14 in FIG. 8 of Boerstler depicts "an input node for receiving the clock signal" as recited in Applicant's claim 1. Reference character 14 does *not* correspond to an input node but rather to a "D-type multiphase detector" that receives an input *data signal*, and a plurality of clock signals derived from the *data signal.* Further, the Examiner indicates that reference character 16 in FIG. 8 corresponds to "a process clock signal" as recited in claim 1. Reference character does not correspond to "a process clock signal" but rather to a charge pump: "Charge-pump 16 creates a control (feedback) voltage for VCO 12 from the error signal." (Boerstler application, Paragraph 51).

Accordingly, the Boerstler application simply does not disclose the subject matter of claim 1 for which it is cited. In addition, to continue to rely on the Boerstler application would violate the guidelines provided in MPEP § 2143.01 which require that the proposed combination cannot change the principle of operation of the reference. In fact, Applicant does not understand how it can be meaningfully said that the Boerstler circuit depicted in FIG. 8 can be modified to give rise to Applicant's invention since the Boerstler circuit is intended for use on a different input (a data signal) and operates in a totally different manner to achieve different results. The purported "modification" of Boerstler would, in fact, be by necessity a wholesale redesign guided by teachings only found in Applicant's disclosure. This is by definition improper hindsight.

The Harrison patent adds nothing to overcome the deficiencies of the Boerstler application.

In conclusion, Applicant respectfully submits that in light of the foregoing arguments claim 1 is patentable over the art of record. Applicant therefore respectfully requests that the rejection of independent claim 1 be withdrawn. Applicant respectfully submits that claim 5 is patentable for reasons similar to those set forth with respect to claim 1 and for reasons attributable to the unique features of claim 5. As a result, Applicant respectfully requests that the rejection of claim 5 be withdrawn as well. Claims 2, 6 and 8 are allowable as depending from allowable base claims.

B. Rejection of Claims 3 and 7 under 35 U.S.C. § 103(a)

Applicant respectfully submits that claims 3 and 7 are patentable as depending directly on allowable base claims. For this reason, and for reasons associated with their unique feature, Applicant respectfully request that the rejection of claim 3 and 7 be withdrawn.

III. Conclusion

The Applicant submits that in light of the foregoing remarks the application is now in condition for allowance. Applicant therefore respectfully requests that the outstanding rejections be withdrawn and that the case be passed to issuance.

Respectfully submitted,

October 28, 2005
Date

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